MC74VHCT393A

Advance Information

Dual 4-Bit Binary Ripple Counter

The MC74VHCT393A is an advanced high speed CMOS dual 4–bit binary ripple counter fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

This device consists of two independent 4–bit binary ripple counters with parallel outputs from each counter stage. A ÷256 counter can be obtained by cascading the two binary counters.

Internal flip–flops are triggered by high–to–low transitions of the clock input. Reset for the counters is asynchronous and active–high. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the VHC393.

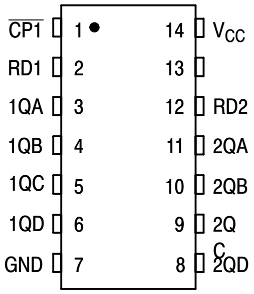
The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V because it has full 5 V CMOS level output swings.

The VHCT393A input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. The output structures also provide protection when $V_{CC} = 0$ V. These input and output structures help prevent device destruction caused by supply voltage—input/output voltage mismatch, battery backup, hot insertion, etc.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output., The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.

- High Speed: f_{max} = 170MHz (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- TTL–Compatible Inputs: V_{IL} = 0.8 V; V_{IH} = 2.0 V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.8V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

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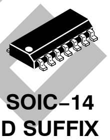
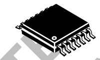
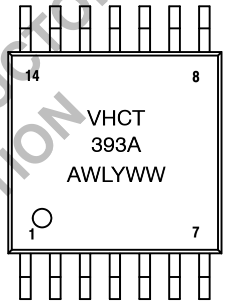
MARKING DIAGRAMS



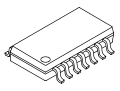
SOIC–14
D SUFFIX
CASE 751A



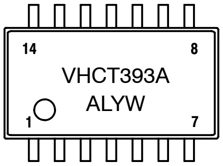
TSSOP–14
DT SUFFIX
CASE 948G



A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week



SOIC EIAJ–14
M SUFFIX
CASE 965

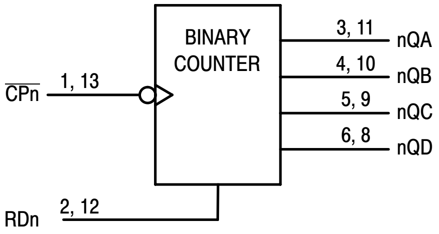


A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74VHCT393AD	SOIC–16	55 Units/Rail
MC74VHCT393ADR2	SOIC–16	1000 Units/Reel
MC74VHCT393ADT	TSSOP–16	96 Units/Rail
MC74VHCT393ADTR2	TSSOP–16	2500 Units/Reel
MC74VHCT393AM	SOIC EIAJ–16	50 Units/Rail
MC74VHCT393AMEL	SOIC EIAJ–16	2000 Units/Reel

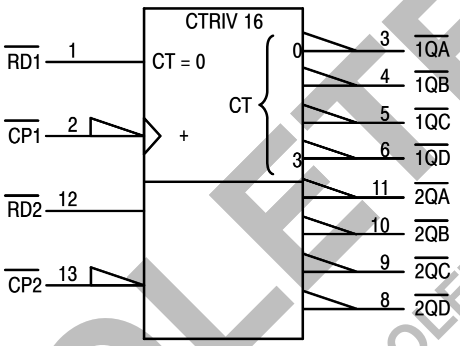
LOGIC DIAGRAM



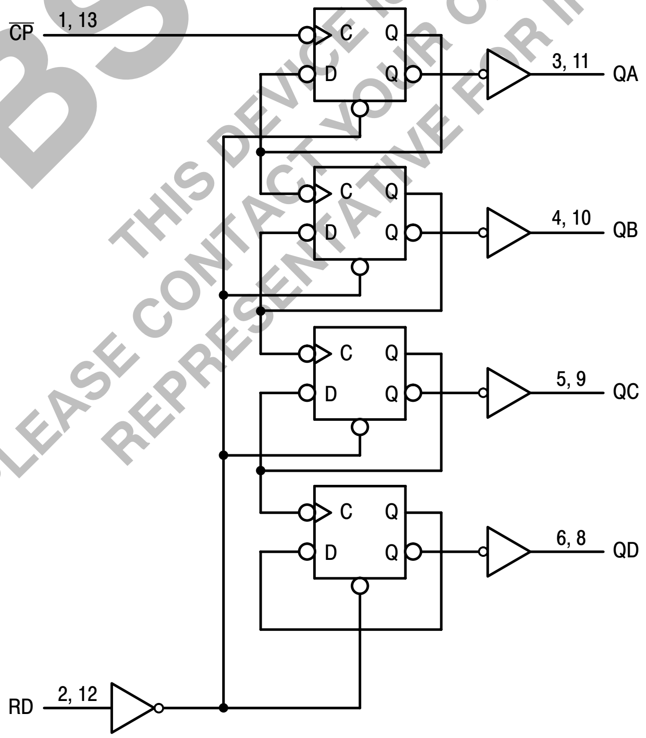
FUNCTION TABLE

Inputs		Outputs
Clock	Reset	
X	H	L
H	L	No Change
L	L	No Change
↑	L	No Change
↓	L	Next State

IEC LOGIC SYMBOL



EXPANDED LOGIC DIAGRAM



MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{IN}	DC Input Voltage	– 0.5 to + 7.0	V
V_{OUT}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{OUT}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	5.5	V
V_{IN}	DC Input Voltage	0	5.5	V
V_{OUT}	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	– 55	+ 125	°C
t_r, t_f	Input Rise and Fall Time V_{CC} = 5.0 V ± 0.5 V	0	20	ns/V

The θ_{JA} of the package is equal to 1/Derating. Higher junction temperatures may affect the expected lifetime of the device per the table and figure below.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

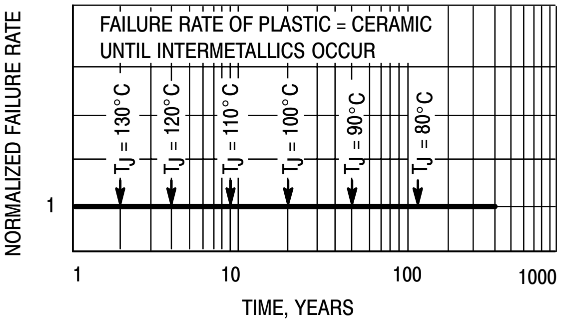


Figure 1. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	T_A = ≤ 85°C Min	T_A = ≤ 85°C Max	T_A = ≤ 125°C Min	T_A = ≤ 125°C Max	Unit
V_{IH}	Minimum High−Level Input Voltage		3.0 4.5 5.5	1.2 2.0 2.0			1.2 2.0 2.0		1.2 2.0 2.0		V
V_{IL}	Maximum Low−Level Input Voltage		3.0 4.5 5.5			0.53 0.8 0.8		0.53 0.8 0.8		0.53 0.8 0.8	V
V_{OH}	Minimum High−Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OH} = − 50 μA	3.0 4.5	2.9 4.4	3.0 4.5		2.9 4.4		2.9 4.4		V
		V_{IN} = V_{IH} or V_{IL} I_{OH} = −4 mA I_{OH} = −8 mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
V_{OL}	Maximum Low−Level Output Voltage V_{IN} = V_{IH} or V_{IL}	V_{IN} = V_{IH} or V_{IL} I_{OL} = 50 μA	3.0 4.5		0.0 0.0	0.1 0.1		0.1 0.1		0.1 0.1	V
		V_{IN} = V_{IH} or V_{IL} I_{OL} = 4 mA I_{OL} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I_{IN}	Maximum Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			2.0		40.0		40.0	μA
I_{CCT}	Quiescent Supply Current	Input: V_{IN} = 3.4 V	5.5			1.35		1.50		1.50	mA
I_{OPD}	Output Leakage Current	V_{OUT} = 5.5 V	0.0			0.5		5.0		5.0	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 ns)

Symbol	Parameter	Test Conditions		T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	T_A = ≤ 85°C Min	T_A = ≤ 85°C Max	T_A = ≤ 125°C Min	T_A = ≤ 125°C Max	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle)	V_{CC} = 3.3 ± 0.3 V	C_L = 15pF C_L = 50pF	75 45	120 65		65 35		65 35		MHz
		V_{CC} = 5.0 ± 0.5 V	C_L = 15pF C_L = 50pF	125 85	170 115		105 75		105 75		
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{CP}$ to QA	V_{CC} = 3.3 ± 0.3 V	C_L = 15pF C_L = 50pF		8.6 11.1	13.2 16.7	1.0 1.0	15.5 19.0	1.0 1.0	15.5 19.0	ns
		V_{CC} = 5.0 ± 0.5 V	C_L = 15pF C_L = 50pF		5.8 7.3	8.5 10.5	1.0 1.0	10.0 12.0	1.0 1.0	10.0 12.0	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{CP}$ to QB	V_{CC} = 3.3 ± 0.3 V	C_L = 15pF C_L = 50pF		10.2 12.7	15.8 19.3	1.0 1.0	18.5 22.0	1.0 1.0	18.5 22.0	ns
		V_{CC} = 5.0 ± 0.5 V	C_L = 15pF C_L = 50pF		6.8 8.3	9.8 11.8	1.0 1.0	11.5 13.5	1.0 1.0	11.5 13.5	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{CP}$ to QC	V_{CC} = 3.3 ± 0.3 V	C_L = 15pF C_L = 50pF		11.7 14.2	18.0 21.5	1.0 1.0	21.0 24.5	1.0 1.0	21.0 24.5	ns
		V_{CC} = 5.0 ± 0.5 V	C_L = 15pF C_L = 50pF		7.7 9.2	11.2 13.2	1.0 1.0	13.0 15.0	1.0 1.0	13.0 15.0	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, $\overline{CP}$ to QD	V_{CC} = 3.3 ± 0.3 V	C_L = 15pF C_L = 50pF		13.0 15.5	19.7 23.2	1.0 1.0	23.0 26.5	1.0 1.0	23.0 26.5	ns
		V_{CC} = 5.0 ± 0.5 V	C_L = 15pF C_L = 50pF		8.5 10.0	12.5 14.5	1.0 1.0	14.5 16.5	1.0 1.0	14.5 16.5	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$			$T_A = \leq 85°C$		$T_A = \leq 125°C$		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PHL}	Maximum Propagation Delay, RD to QN	$V_{CC} = 3.3 \pm 0.3$ V	$C_L = 15pF$ $C_L = 50pF$		7.9 10.4	12.3 15.8	1.0 1.0	14.5 18.0	1.0 1.0	14.5 18.0	ns
		$V_{CC} = 5.0 \pm 0.5$ V	$C_L = 15pF$ $C_L = 50pF$		5.4 6.9	8.1 10.1	1.0 1.0	9.5 11.5	1.0 1.0	9.5 11.5	ns
t_{OSLH}, t_{OSHL}	Output to Output Skew	$V_{CC} = 3.3 \pm 0.3$ V (Note 1)	$C_L = 50pF$			1.5		1.5		1.5	pF
		$V_{CC} = 5.0 \pm 0.5$ V (Note 1)	$C_L = 50pF$			1.0		1.0		1.0	pF
C_{IN}	Maximum Input Capacitance				4	10		10		10	pF

		Typical @ 25°C, $V_{CC} = 5.0V$	
C_{PD}	Power Dissipation Capacitance (Note 2)	23	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 5.0$V)

Symbol	Parameter	$T_A = 25°C$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	− 0.5	− 0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions	$T_A = 25°C$		$T_A = \leq 85°C$	$T_A = \leq 125°C$	Unit
			Typ	Limit	Limit	Limit	
t_w	Minimum Pulse Width, $\overline{\text{CP}}$	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V		5.0 5.0	5.0 5.0	5.0 5.0	ns
t_w	Minimum Pulse Width, RD	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V		5.0 5.0	5.0 5.0	5.0 5.0	ns
t_{rec}	Minimum Recovery Time, RD to $\overline{\text{CP}}$	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V		5.0 4.0	5.0 4.0	5.0 4.0	ns
t_r, t_f	Minimum Input Rise and Fall Times	$V_{CC} = 3.3 \pm 0.3$ V $V_{CC} = 5.0 \pm 0.5$ V		330 100	330 100	330 100	ns

SWITCHING WAVEFORMS

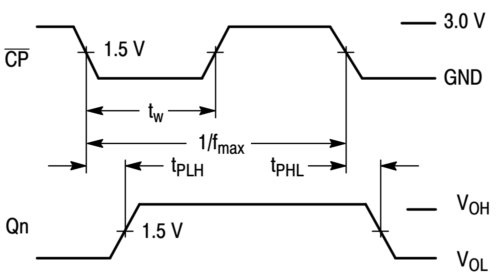


Figure 2.

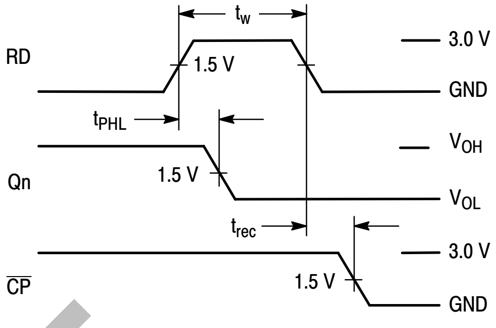
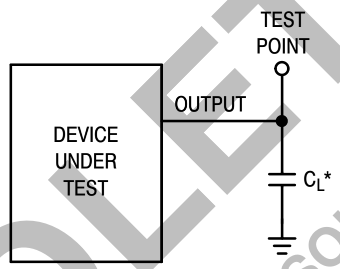


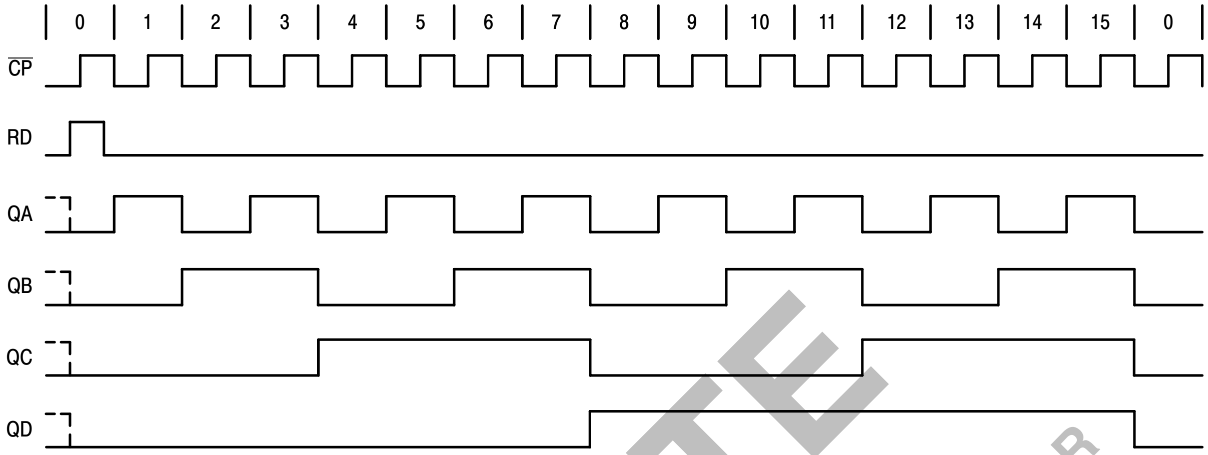
Figure 3.



*Includes all probe and jig capacitance

Figure 4. Test Circuit

TIMING DIAGRAM

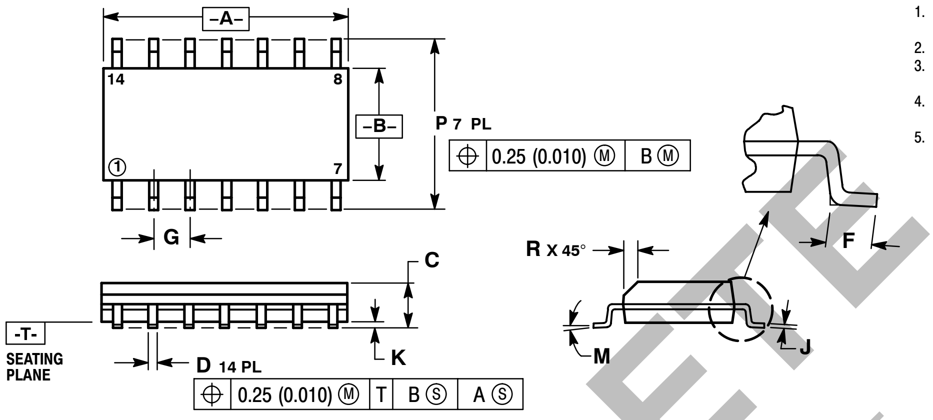


COUNT SEQUENCE

Count	Outputs			
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

PACKAGE DIMENSIONS

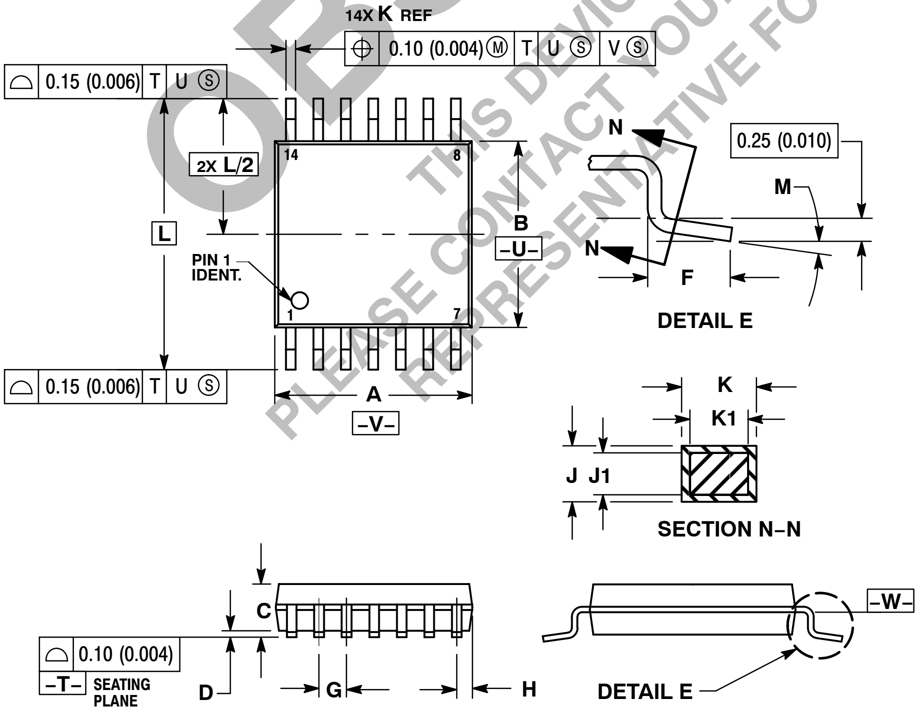
SOIC−14
D SUFFIX
CASE 751A−03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

TSSOP−14
DT SUFFIX
CASE 948G−01
ISSUE O

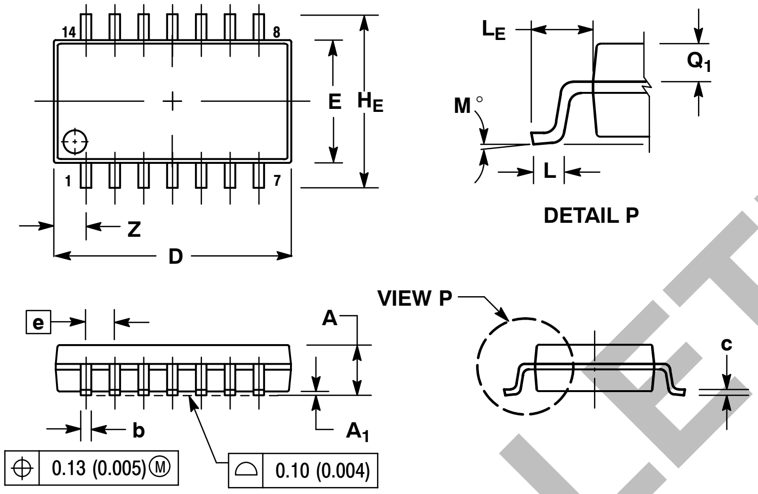


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

PACKAGE DIMENSIONS

SOIC EIAJ−14
M SUFFIX
CASE 965−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

OBSOLETE
THIS DEVICE IS OBSOLETE
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